Position Description: Manager/Sr/Staff/Sr Staff IC Design Engineer

Location: Tainan (preferred)/Nangang/Chubei (preferred), Taiwan

Manager/Senior/Staff/Senior Staff Design Engineer

Manager: High skill involved technical and management a small team. Able to work independent and supervise/recruit the design team member.

Staff Design Engineer: Perform independent integrated circuit design, simulation and verification for design using CMOS technology with little or no supervision.

Principle Duties and Responsibilities:

- Work as a key member in a development team, perform analog/mixed signal circuit design and design verification using deep submicron CMOS process technology. The individual need to carry out assigned circuit design independently and mentor junior engineer, need to supervise layout work and working with product engineering and test engineering for post silicon verification and product characterization.
- The individual needs to define circuit structures and product architecture, need to carry the design from front end concept to back end physical implementation, and he/she is able to generate high level product model and provide occasional customer support.
- Responsible for analog and mixed signal design and knowledgeable on analog building blocks, PLLs (LC tank with 10 GHz or above in deep submicron process such as 14-28 nm), DFE/CTLE, digital filter, I/O structure and ESDs
- The individual needs to work with digital team and define the signals between analog and digital interface and make sure the quality of final digital delivery
- The individual is able to create and verify the behavior model in circuit/system design
- The individual need to create and maintain documentation for the related project work and may create and improve the design flow

Knowledge, Skills and Abilities:

- MSEE/PhD with a minimum 0-10 years' experience or BSEE with 2-10 years' experience. MS or PhD preferred.
- Requires analog and mixed signal integrated circuit design experience, familiar with SERDES, PLL, and DFE/CTLE designs, Gigabit per second serial link design is preferred.
- Knowledge in Cadence tool set, Synopsys tool set, hspice simulation tool, Verilog simulation, Matlab, and layout tools.
- Ability to work as a team and able to work across other groups.

For more information, please visit the website: https://www.diodes.com/tw/

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職務說明書 Job Description

職務 Position:	Analog IC Design Manager	部門 Dept.	Analog LLP RD
聘任性質 Character:	■正職 Regular □約聘 Temporary □Full Time □Part Time	HC Status	New, apr date:____ASAP____. □Replace:
直屬主管 Reports to:	Leo Cho	上班地點 Location:	Tainan Office

I.職務條件 Position Requirements	
1.學歷科系 Education:	BSEE or above
2.工作經歷 Employment Experience:	■ 7 年以上相關經驗 ■ 2 年以上部門主管經驗 □專案經驗
3.語言能力 Language level:	■English, level Fair ability to communicate in spoken and written English □Other:_____level _____.
4.人格特質 Personality:	Integrity, taking ownership
5.專業證照 Certification:	Not specified
6.電腦技能 Computer Skills:	1. Composer/Virtuoso/Spectre of Cadence; 2. HSpice/Finesim of Synopsys 3. Microsoft Office 4. Unix/Linux
II.組織中之從屬關係 Reporting Line	
III.工作內容 Description of Duties	
1. Develop and lead a team for power IC for automotive, industry and consumer applications. 2. Responsible for part definition, design, simulation, analysis and documentation 3. Work with and provide guidance to layout engineers and monitor the progress of IC layout 4. Collaborate with validation, product and test engineering teams to enable successful transfer parts to production 5. Strive and promote continuous improvements to ensure the quality and competitiveness of our products. 6. Lead and drive design team to build parts meeting cost and performance requirements on time 7. Recruit and mentor people in technical execution and project coordination including MKT, PTE, QRA etc	
IV.其他 Additional Requirements(ex:tool, software,industry, etc.)	
Indispensable skill: 1. In depth working experience with Composer/Virtuoso/Spectre of Cadence or HSpice/Finesim of Synopsys 2. Experience in lab measurement and equipment, such as oscilloscope, and hands-on soldering skills. 3. Strong verbal and written communication skills 4. Strong time management skills that enable on-time project delivery Professional knowledge 1. Comprehension of analog circuit theory, layout pitfalls, and proven capability in problem solving are essential. Prior experience or knowledge of high-voltage circuit design or power supply regulators (LDO and DC/DC) is a plus. 2. Working knowledge of semiconductor devices and process technologies.	

Remark:
When hiring manager filled out this form. HR will help to fill ER form from EIP flow accordingly.
ER No.:_____ New Hired Name:_____ On board date:_____.

JD provided by:_____ , version by:_____, Posted 104: